

5 a first conductive material positioned on said at least one internal side wall of said
6 substrate;

7 a first conductive layer positioned on a portion of said first surface of said substrate, said
8 first conductive layer having a first layer portion positioned over said through hole, said first
9 layer portion electrically connected and sealed to said first conductive material on said internal
10 side wall of said substrate by a first metallurgical diffusion bond;

11 a second conductive layer positioned on a portion of said second surface of said substrate,
12 said second conductive layer having a first layer portion positioned over said through hole, said
13 first layer portion electrically connected and sealed to said first conductive material on said
14 internal side wall of said substrate by a second metallurgical diffusion bond;

15 a first dielectric layer positioned on said first conductive layer and said first opposing
16 surface of said substrate and having at least one internal side wall defining an aperture in said
17 first dielectric layer; and

18 a second conductive material positioned on said internal side wall of said first dielectric
19 layer and including a portion of said second conductive material positioned on and electrically
20 connected to said first layer portion of said first conductive layer.

1 22. The interconnect structure of claim 21, further including a chip connector member having a
2 portion thereof positioned on said second conductive material.

1 23. An interconnect structure comprising:

2 a substrate having first and second opposing surfaces and at least one internal side wall
3 defining a through hole within said substrate extending from said first opposing surface to said
4 second opposing surface, wherein said substrate includes a metal layer between said first and
5 second opposing surfaces and first and second non-conductive layers positioned, respectively,
6 between said first opposing surface and said metal layer and between said second opposing
7 surface and said metal layer;

8 a third conductive layer positioned substantially within said first non-conductive layer;

9 a fourth conductive layer within said first non-conductive layer and positioned between
10 said third conductive layer and said metal layer;

11 a first conductive material positioned on said at least one internal side wall of said
12 substrate;

13 a first conductive layer positioned on a portion of said first surface of said substrate, said
14 first conductive layer having a first layer portion positioned over said through hole and
15 electrically connected to said first conductive material on said internal side wall of said substrate;

16 a second conductive layer positioned on a portion of said second surface of said substrate,
17 said second conductive layer having a first layer portion positioned over said through hole and
18 electrically connected to said first conductive material on said internal side wall of said substrate;

19 a first dielectric layer positioned on said first conductive layer and said first opposing
20 surface of said substrate and having at least one internal side wall defining an aperture in said
21 first dielectric layer; and

22 a second conductive material positioned on said internal side wall of said first dielectric
23 layer and including a portion of said second conductive material positioned on and electrically
24 connected to said first layer portion of said first conductive layer.

1 24. The interconnect structure of claim 23, wherein said metal layer is selected from the
2 group consisting of nickel, copper, molybdenum, iron, and alloys thereof.

1 25. The interconnect structure of claim 23, wherein said metal layer comprises copper-Invar-
2 copper.

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1 26. The interconnect structure of claim 23, wherein said fourth conductive layer comprises a
2 first plurality of controlled impedance signal conductors.

1 27. The interconnect structure of claim 23, further including a fifth conductive layer
2 positioned substantially within said second non-conductive layer.

1 28. The interconnect structure of claim 27, further including a sixth conductive layer
2 positioned substantially within said second non-conductive layer and also positioned
3 substantially between said fifth conductive layer and said metal layer.

1 29. The interconnect structure of claim 28, wherein said sixth conductive layer comprises a
2 second plurality of controlled impedance signal conductors.--